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AN ULTRA-LOW-POWER 12T CAM CELL BASED ON THRESHOLD VOLTAGE TECHNIQUES

HARIHARAN K[1], RAAJAN N.R[2], MANIKANDAN.R[3] & R.VENKATESAN[4]

[1,3,4] *Assistant Professor, School of Computing, SASTRA University, India*

[2] *Senior Assistant Professor, SEEE, SASTRA University, India*

ABSTRACT

This paper exhibits Thirteen-transistor (12T) CAM cell working in the subthreshold area. In the proposed 12T CAM cell, an appropriate read operation is given by stifling the channel actuated boundary bringing down impact and controlling the body source voltage power. Appropriate utilization of low-edge voltage (LVt) transistors in the proposed plan lessens the read access time and upgrades the dependability in the subthreshold area. In the proposed cell, a typical piece line is utilized in the read and composes operations. This configuration prompts a bigger compose edge without utilizing additional circuits. The recreation results of 90nm CMOS innovation illustrate a qualified execution of the proposed CAM cell regarding power scattering, power delay item, compose edge, read access time and affect the ability to process, voltage furthermore, temperature varieties when contrasted with the other most effective low-voltage CAM cells beforehand introduced in the writing mode.

KEYWORDS: CAM, Ultra Low Power, Threshold Techniques & Power Optimization

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Original Article

INTRODUCTION

These days, ultra-low-control circuit outline assumes a significant part in vitality basic applications. Low-control outline methods include distinctive levels, for example, framework, register exchange rationale (RTL), circuit and gadget [1]. The execution necessities for miniaturized scale and nano-sensors, in low-control circuits are restricted. Be that as it may, micro and nano-sensor hub applications require long battery lifetimes, as it is difficult to energize or supplant batteries oftentimes. Besides, most compact electronic gadgets utilized for applications require a low-control computerized signal processor (DSP) or microcontroller unit (MCU). What's more, inquires about have shown that, the base vitality point (MEP) can be accomplished in the subthreshold district. In other words, proper power delay item (PDP) can be found in the close subthreshold district [3]. CAMs involve a noteworthy part of the territory and expend a lot of force in electronic chips. Therefore, control diminishment in CAM exhibits is a primary issue in low-control VLSI outline. A direct system for diminishing the static streams, what's more, power scattering is lessening the supply voltage (VDD) [1]. Be that as it may, the effect of procedure varieties turns out to be more concentrated in little size gadgets with lower supply voltages, and it turns out to be even exponential in the subthreshold area [3]. Plus, expanding irregular dopant limit voltage (Vt) varieties, can prompt considerable disappointments in CAM cells [5]. Expanding spillage streams are another impact of Vt variety, as spillage streams are exponentially expanded by lessening the limit voltage. Power utilization of CAM, affects the aggregate force devoured in computerized incorporated circuits. As CAM cells are regularly in the hold state, lessening the static force dispersal of CAM cells, fundamentally decreases the aggregate

force utilization.

THE PROPOSED DESIGN OF A CAM CELL

The proposed outline of a 12T CAM cell appears in Figure 2. In the proposed outline, the proficiency of the read operation at low voltages is accomplished by using a double Vt method, which improves the ION/IOFF proportion. As shown in Figure 5, the wellspring of M8 and the gate of M7, L-Vt transistors are associated with the read word-line (RWL). Accordingly, amid the perused operation, when RWL is changed to zero, accepting that hub QB voltage is high, pre-charged piece line (BLB) is released to ground through the L-Vt transistors (M7 what's more, M8). Along these lines, the releasing current of the pre-charged piece line is fundamentally expanded, an appropriate condition for reading operation at ultra-low voltages. As the read current improves, the entrance time is diminished. In any case, in the past plans, the perused access time increments at ULV because of a feeble read current. Then again, in the hold state when RWL is high (VDD), the IOFF of the read way is right around zero worth. Assume that, the put away information at hub QB is "1." Thus, the channel voltage of M8 transistor is "1." subsequently, the drain source voltages of M8 and M7 transistors are zero which stifle the DIBL impact and subsequently build the limit voltage of M8 and M7. Likewise, the high voltage of the source hub and the

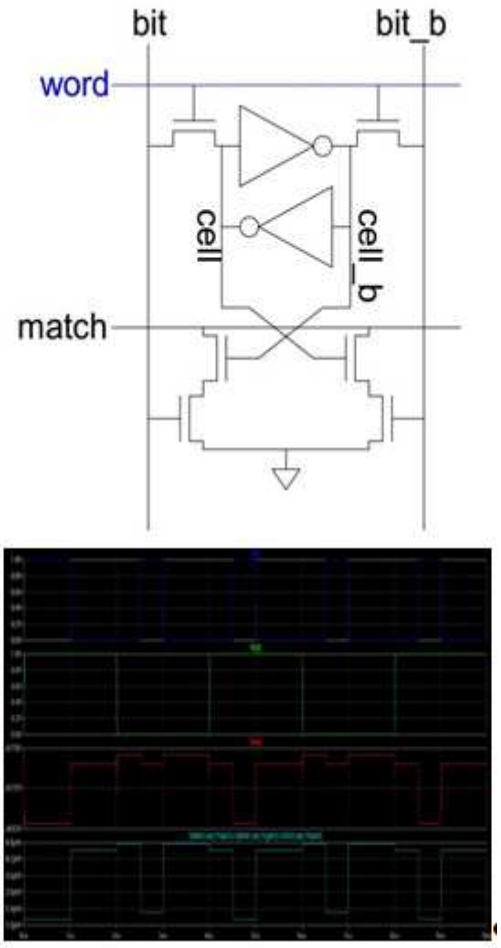

Figure 1: Traditional Design and Waveform

The Zero voltage of the body hub (VBS = VDD) expands the Vt of M8. Therefore, the force utilization and the spillage current on the readout way are diminished altogether, when the CAM cell is in the hold state. In addition, the PN-

intersection diode of the body source is in a safe switched inclination. Moreover, in the proposed structure, when the voltage of hub Q is high, by lessening the quality of the draw up M9 transistor inside, the compose edge (WM) is expanded and the aggregate static current is lessened. The gate width of all transistors aside from the entrance transistors (M5 and M2) are set to 120nm, the base conceivable gate width of the innovation. The

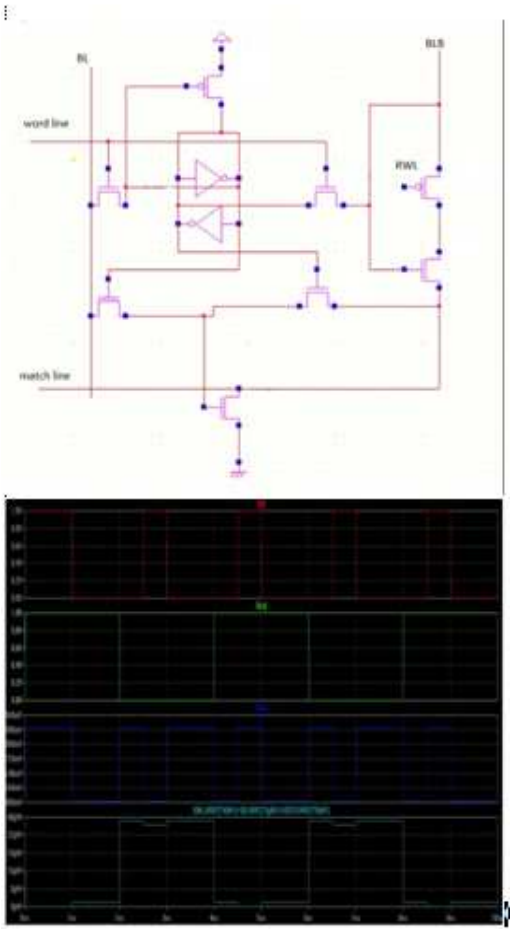

Figure 2: Proposed Design and Waveform

Widths of M2 furthermore, the M5 is received as 240nm to build the compose dependability [5]. Also, the entryway lengths of all transistors are embraced as 100nm which is the base conceivable gate length of the innovation. The compose operation is performed by driving the differential compose bit-lines (BL also, BLB) to the level of the information to be composed and enacting the compose word-line (WWL). To guarantee the achievement of this operation in the cells, the draw down NMOS transistor must beat the draw up PMOS transistor. The electron portability is higher than the gap versatility. Be that as it may, at low voltages close to the edge voltage, the huge current change, brought on by procedure varieties, frequently upsets scrutinizing the draw pMOS transistors, proportionate to the nMOS access transistors. In the proposed cell, the criticism circle from hub Q to the entryway of M9 transistor together with embracing the size of access transistors enhances the compose clamor edges. The embraced size of the entrance transistors is thought to be two times the measure of draw up transistor. For a CAM cell, static force utilization is a noteworthy concern. Spillage streams are expanded in the hold ”1” state for M1 (VGS = 0, VDS = VQ) and in the hold ”0” state, for M4 (VGS = 0, VDS = VQB) by DIBL. Keeping in mind the end goal to relieve this issue, the sizes of the draw down transistors (M1, M4) are received as the base conceivable size of the innovation. The proposed 12T CAM accomplishes the

accompanying commitments: Static force lessening through M7 and M8 by using progressively controlled source body voltage and smothered DIBL impact, Static force lessening through M9 by supply voltage gating in the hold"1" state what's more, its stacking impact in the hold"0" state, Read access time decrease by using L-Vt transistors and reasonable at ULV, The WM change of the CAM cell, Energy utilization decrease, PVT variety decrease.

Read and Write Operations

In outlining low-voltage CAMs, security of the read and compose operations is a vital parameter. A legitimate configuration can diminish the quantity of disappointments in a CAM cell, including reading, composes and get to time disappointments [5]. It merits saying that the most intriguing issue in the proposed CAM cell is its execution amid a perused/compose operation and its hold state.

Read Operation

A critical measure in CAM cell is the perused current, as it decides the read speed [1]. The read access time relies on upon some outline variables, for example, principally bit-line capacitance, affectability of sense intensifier and drive quality of read cradle transistors (M7 and M8 in Figure 5). In this work, the read operation is enhanced by using L-Vt transistors (M7 and M8) in the readout way to diminish the read access time. Additionally, with this method, the read operation is performed dependably at ULVs. In view of utilizing L-Vt transistors (M7 and M8) in the proposed outline, the readout way resistance gets to be littler. Thusly, in the CAM cell, the rate of releasing the BLB to ground through the readout way is upgraded. Assume that, a"1" information is put away on the QB. At the point, when the read word-line (RWL) changes to zero, read operation begins. Along these lines, the M7 and M8 transistors turn ON, changing RWL to zero prompts expanding the VDS of M8 and M7. The Vt voltages of M8 and M7 transistors, diminish further. In this manner, the BLB begins to release by means of L-Vt transistors. By releasing BLB, the voltage contrast amongst BLB and BL is detected by sense intensifier. The rapid and adequate releasing of pre-charged piece line (BLB), result in a solid read operation even at ULV. What's more, affect the ability of the configuration structure of the sense intensifier is diminished. The estimations of the read streams and read access time varieties at various procedure corners and temperatures are talked about in the reproduction results segment.

Write Operation

The compose operation of the proposed cell is like the 12T cell introduced in [4]. On this phone, an inward debilitating of the draw up current amid the compose cycles empowers low-voltage compose operations. Amid the compose operation, the static compose dependability or static compose edge metric is characterized as the contrast amongst VDD and WWL voltage when the hubs Q and QB flip [16]. This methodology clears the voltage of WL on both sides at the same time to give a genuine compose operation. To expand the compose solidness, the entrance transistors should be reinforced, while the draw up transistors ought to be debilitated. In this work, so as to have the solid compose operation, the width of access transistors (M2 and M5) is embraced two times bigger than the draw up pMOS transistors (M3 and M6) [3]. Additionally, the proposed structure has bigger WM when contrasted with the 10T and 12T [8] cells. On the off chance that, the put away information (on Q) are "0," for composing "1," BLB is released to GND and BL is charged to VDD. As indicated by the planning graph of the proposed CAM (see Fig. 6) in the compose interim, WWL changes to VDD. Thus, M2 turns ON and therefore, the hub QB is released to the grounded BLB bit-line. On the off chance that, the voltage of QB does not diminish beneath the excursion point (Vtrip) of the inverter (M3 and M1), a

compose disappointment happens. As indicated by Figure 5, charging the voltage of the hub Q into ”1” debilitates the M9 transistor. By debilitating the M9 transistor, M5 overcomes M6 and releases the hub QB and hence WM improves.

For composing”0” on Q, BLB is charged to VDD and BL is released to GND. The voltage of WWL changes from GND to VDD, and the compose operation begins. They put away information at the hub Q release to GND through M2 transistor. Releasing Q turns the M9 and M6 transistors ON and consequently QB charges to VDD. Subsequently, the compose edges of the proposed structure are bigger than the compose edges of the 10T and 12T cells and close to the 12T cell off. The estimations of compose”0” and”1” edges of the proposed plan and the 10T and 12T CAM cells are accounted for in the Order. 5.

CONCLUSIONS

In this paper, a low-power and PVT-tolerant sub threshold 12T CAM cell was displayed. Powerful methods taking into account progressively controlled source body voltage furthermore, DIBL impact for the readout way transistor furthermore a stacked pMOS gadget was used to keep in mind the end goal to decrease the force utilization, in the hold state and enhance the execution of the read operation. Those accomplishments were acquired, without using any fringe circuits and expanding the span of the transistors. Since, littler spillage streams expand information stockpiling strength, in short-channel gadgets, solid CAMs can be outlined utilizing the proposed bit-cell. The recreation results in light of 90nm CMOS innovation affirmed the predominance of the proposed cell. At low voltages, the proposed cell gave optimum results.

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